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To: LSC members
(transmitted via email through the LSC chairman, Peter Saulson)
From: Rolf Bork, Dennis Coyne
Subject: Data Acquisition Errors on LHO4k and LHO PEM

Revision 02:
(i) Corrected the list of channels. The list in revision –01 was incomplete.
(ii) Added a note regarding the effect on the RDSs.

During recent signal injection testing, a problem was noted with data from two Analog Data Collection Units (ADCU) (specifically h1adcusus and h1adcupem). This was subsequently tracked down to a software problem in these two ADCU. These two ADCU are different than all others in LIGO in that they are the only two directly connected to the framebuilder network.

The problem originated when the framebuilder network at Hanford was switched over to a newer high speed network back in January. The new net was installed to accommodate the high data load. The older network cards had hardware byte swapping (needed to send data from a Pentium to the Sun), but the new network boards do not have this feature. Therefore, the software was changed in these ADCU to do the byte swapping. Unfortunately, it was not noted that while the ADCU writes the data as shorts, the framebuilder, using 32 bit DMA to receive the data, actually reads integers. This results in improper byte swapping.

The net result in the stored data frames is that data samples for these two ADCU are correct in value but out of time order. So the time series, from the beginning of a frame, instead of being (S)ample 0, S1, S2, S3, S4, ..., got stored as S1,S0,S3,S2,S5,S4 .... i.e. pairs of data samples are swapped in the time series. There are 152 effected channels (listed below). The channels include some LHO Physics Environment Monitoring (PEM) channels as well as some auxiliary 4 km interferometer channels. Some of these channels might be used in veto analysis.

The framebuilder software was corrected, reloaded and tested 7/30 (the error existed from 1/6 through 7/29). Unfortunately, the S2 data has this swapped sample problem. The LIGO Lab LDAS group feels that it would not be appropriate to correct this problem in the raw data; If an error occurs in the correction, then the archives might get corrupted and require fixes upon fixes. As a consequence the tools used to do the data analysis must recognize and correct the problem. We apologize for the resulting impact on the data analysis tools, the awkwardness of this solution and any inconvenience this error may cause you.

The high speed channels in the Reduced Data Sets (RDSs) were first down-sampled and then decimated. Such channels contain incorrect time series data that cannot be corrected,

thus leading to the possible need to regenerate S2 RDSs if these channels are required. This is a significant undertaking. Moreover the capability to swap samples on selected channels does not exist in the current RDS software. Because this was discovered well into the software development cycle for S3 release, unfortunately, it cannot be developed and validated in parallel with efforts to support the S3 run.

The LIGO Laboratory is reviewing its procedures and policies with regard to the real time software quality assurance and will be making changes to reduce the risk of such errors in the future.

Effected channels: Derived from Run1707 (13 Feb 2003). This is the definitive S2 master.config file defined one day before S2 started and maintained throughout the S2 run.

H1:SUS-RM_COIL_UL	H1:SUS-RM_COIL_LL	H1:SUS-RM_COIL_UR
H1:SUS-RM_COIL_LR	H1:SUS-RM_COIL_SIDE	H1:SUS-BS_COIL_SIDE
H1:SUS-BS_COIL_UL	H1:SUS-BS_COIL_LL	H1:SUS-BS_COIL_UR
H1:SUS-BS_COIL_LR	H1:SUS-ITMX_COIL_UL	H1:SUS-ITMX_COIL_LL
H1:SUS-ITMX_COIL_UR	H1:SUS-ITMX_COIL_LR	H1:SUS-ITMX_COIL_SIDE
H1:SUS-ITMY_COIL_SIDE	H1:SUS-ITMY_COIL_UL	H1:SUS-ITMY_COIL_LL
H1:SUS-ITMY_COIL_UR	H1:SUS-ITMY_COIL_LR	H1:SUS-MMT3_COIL_UL
H1:SUS-MMT3_COIL_LL	H1:SUS-MMT3_COIL_UR	H1:SUS-MMT3_COIL_LR
H1:SUS-MMT3_COIL_SIDE	H1:SUS-MC1_COIL_UL	H1:SUS-MC1_COIL_LL
H1:SUS-MC1_COIL_UR	H1:SUS-MC1_COIL_LR	H1:SUS-MC1_COIL_SIDE
H1:SUS-MC2_COIL_UL	H1:SUS-MC2_COIL_LL	H1:SUS-MC2_COIL_UR
H1:SUS-MC2_COIL_LR	H1:SUS-MC2_COIL_SIDE	H1:SUS-MC3_COIL_UL
H1:SUS-MC3_COIL_LL	H1:SUS-MC3_COIL_UR	H1:SUS-MC3_COIL_LR
H1:SUS-MC3_COIL_SIDE	H1:SUS-SM_COIL_UL	H1:SUS-SM_COIL_LL
H1:SUS-SM_COIL_UR	H1:SUS-SM_COIL_LR	H1:SUS-SM_COIL_SIDE
H1:SUS-MMT1_COIL_UL	H1:SUS-MMT1_COIL_LL	H1:SUS-MMT1_COIL_UR
H1:SUS-MMT1_COIL_LR	H1:SUS-MMT1_COIL_SIDE	H1:SUS-MMT2_COIL_UL
H1:SUS-MMT2_COIL_LL	H1:SUS-MMT2_COIL_UR	H1:SUS-MMT2_COIL_LR
H1:SUS-MMT2_COIL_SIDE	H1:PSL-FSS_FAST_F	H1:PSL-FSS_MIXERM_F
H1:PSL-FSS_RFPDDC_F	H1:PSL-FSS_RCTRANSPD_F	H1:PSL-PMC_ERR_F
H1:PSL-PMC_PZT_F	H1:PSL-PMC_RFPDDC_F	H1:PSL-PMC_TRANSPD_F
H1:PSL-ISS_SHUNT_AC	H1:PSL-ISS_PDIN_AC	H1:PSL-ISS_PDOUT_AC
H1:PSL-ISS_PDOUT_MON	H1:PSL-ISS_PDIN_DC	H1:PSL-ISS_PDOUT_DC
H1:PSL-TEST1_F	H1:PSL-TEST2_F	H1:IOO-WFS1_P
H1:IOO-WFS1_Y	H1:IOO-WFS2_P	H1:IOO-WFS2_Y
H1:IOO-MC1_P	H1:IOO-MC1_Y	H1:IOO-MC1_REF
H1:IOO-MC2_P	H1:IOO-MC2_Y	H1:IOO-MC2_REF
H1:IOO-WFS1_DCP	H1:IOO-WFS1_DCY	H1:GDS-IRIGB_LVEA
H1:DAQ-GPS_RAMP_L1	H1:LSC-MC_AO	H1:IOO-MC_TO1
H1:IOO-MC_I	H1:IOO-MC_F	H1:IOO-PSL_TEST_MON
H1:IOO-MC_TRANSPD	H1:IOO-MC_REFLPD	H1:GDS-TEST_7_1_18
H1:IOO-MC_TRANSPD_SUM	H1:IOO-MC_TRANSPD_HOR	H1:IOO-MC_TRANSPD_VERT
H1:GDS-TEST_7_1_22	H1:GDS-TEST_7_1_23	H1:LSC-SPOB_MON
H1:LSC-REFL_DC	H1:LSC-POBS_DC	H1:LSC-POY_DC
H1:LSC-AS_AC	H1:LSC-AS_DC	H0:PEM-PSL1_ACCX
H0:PEM-PSL1_ACCY	H0:PEM-PSL1_ACCZ	H0:PEM-HAM1_ACCX
H0:PEM-HAM1_ACCY	H0:PEM-HAM1_ACCZ	H0:PEM-HAM2_ACCX
H0:PEM-HAM2_ACCY	H0:PEM-HAM2_ACCZ	H0:PEM-HAM3_ACCX
H0:PEM-HAM3_ACCY	H0:PEM-HAM3_ACCZ	H0:PEM-HAM4_ACCX
H0:PEM-HAM4_ACCY	H0:PEM-HAM4_ACCZ	H0:GDS-TEST_8_0_15
H0:PEM-BSC2_ACCX	H0:PEM-BSC2_ACCY	H0:PEM-BSC2_ACCZ
H0:PEM-BSC3_ACC1X	H0:PEM-BSC3_ACC1Y	H0:PEM-BSC3_ACC1Z
H0:PEM-BSC3_ACC2X	H0:PEM-BSC3_ACC2Y	H0:PEM-BSC3_ACC2Z
H0:PEM-HAM3_MAGX	H0:PEM-HAM3_MAGY	H0:PEM-HAM3_MAGZ
H0:PEM-BSC1_MAGX	H0:PEM-BSC1_MAGY	H0:PEM-BSC1_MAGZ
H0:PEM-PSL1_MIC	H0:PEM-HAM1_MIC	H0:PEM-HAM2_MIC
H0:PEM-HAM3_MIC	H0:PEM-HAM4_MIC	H0:PEM-BSC2_MIC
H0:PEM-BSC2_MAGX	H0:PEM-BSC2_MAGY	H0:PEM-BSC2_MAGZ
H0:PEM-BSC3_MAGX	H0:PEM-BSC3_MAGY	H0:PEM-BSC3_MAGZ
H0:PEM-LVEA_MAGX	H0:PEM-LVEA_MAGY	H0:PEM-LVEA_MAGZ
H0:PEM-RADIO_CS_1	H0:PEM-RADIO_CS_2	